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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,374	07/08/2003	Jason Bernard Etheridge Julyan	56162.000432	7428

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,374	JULYAN, JASON BERNARD ETHERIDGE	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,15,17,27,28,31 and 33* is/are rejected.

7)☒ Claim(s) *13,14,16,18-26,29,30,32 and 34-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Drawings

2. The preliminary amended drawings were received on 10/09/2003. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

In Figure 1, reference numerals "170", "160", and "197" are not mentioned in the specification.

In Figure 2, reference numerals "214" and "216" are not mentioned in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because in the detailed description of Fig. 1, element "160" –that looks like a multiplexer (possibly the Arithmetic Logic Unit ?) its function is not mentioned. The configuration register element 110 supplies divider values to element 150 ($1/Y_1$ divider) and the DPLL element 190 and controls (?) the multiplexer element 160 to select between the two divided frequencies out of elements 140, 150. The function of the configuration register 110 with respect to elements 150, 160, 190 should be clarified.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21, 25, 37, 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 recites, line 3: "...to modify the value of Y_2" Neither claim 15 nor claim 11 mention a value of Y_2.

Claim 25 depends on 21 and is also rejected.

Claims 37, 40 are also rejected for the same reasons as above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11-12, 15, 27-28, 31 rejected under 35 U.S.C. 103(a) as being unpatentable over Tonks et. al., (U.S. 6,121,816) in view of Usui (U.S. 6,469, 583).

With respect to claim 11, Tonks et. al., discloses: receiving an external reference signal from a source node as an input (see Fig. 3, one signal out of plurality of signals 12 "reference sources") ; inputting the first and second output into an arithmetic logic unit to produce a reference clock signal (see Fig. 3, element 32 , "mux" , signal 34, column 5, lines 50-54)) ; inputting the reference clock signal into a digital phase-locked loop (Fig. 3, signal 34 is input to element 44, clock multiplier, digital PLL, column 6, lines 19-25); providing the digital phase locked loop to lock onto the external reference clock (column 6, lines 19-25).

Tonks et. al. do not expressly teach: generating a first integer and a second integer at a configuration and status register; inputting one generated integer into a first divider, and the other generated integer into a second divider; inputting the received external clock reference signal into the first divider; inputting a high speed bus clock signal into the second divider; dividing the receiving external clock reference signal by the first integer to produce a divided external clock reference; dividing the high speed bus clock signal by the second integer to produce an internal clock reference signal;

In the same field of endeavor, Usui discloses: generating a first integer and a second integer at a configuration and status register (see Fig. 1, registers 108 and 109, column 5, lines 53-56); inputting one generated integer into a first divider (Fig. 1, element 104), and the other generated integer into a second divider (Fig. 1, element 104, where the first and second dividers are the same); inputting the received external clock reference signal into the first divider (Fig. 1 the output of reference oscillator signal 101 is divided by the variable frequency divider 104); inputting a high speed bus clock signal into the second divider (Fig. 1, signal 101); dividing the receiving external clock reference signal by the first integer to produce a divided external clock reference (Fig. 1, output of element 104); dividing the high speed bus clock signal by the second integer to produce an internal clock reference signal (Fig. 1, output of element 104, where the high speed bus clock is the output of oscillator 101).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to apply the teachings of Usui including: generating a first integer and a second integer at a configuration and status register; inputting one generated integer into a first divider and the other generated integer into a second divider inputting the received external clock reference signal into the first divider; inputting a high speed bus clock signal into the second divider; dividing the receiving external clock reference (i.e. one of the reference clock signals 12 shown in Fig. 3 of Tonks et. al.,) signal by the first integer to produce a divided external clock reference; dividing the high speed bus clock signal (one of the reference clock signals shown in Fig. 3 of Tonks et. al.,)) by the second integer to produce an internal clock reference signal, because dividing two of

the reference clocks by integers (stored in a configuration and status register under the control of PLL controller 11 of Usui) so that frequency switching is achieved in relatively short time (Usui, column 3, lines 54-58).

With respect to claim 12, all of the limitations of claim 12 are analyzed above in claim 11 and Usui discloses: wherein the first integer divides the external clock value is N_1, which is selected to be either 1, 256, 193, or 192 (column 6, lines 7-12, the (integer) variable divider is understood to by any integer value including one of the 1, 256, 193, or 192).

With respect to claim 15, all of the limitations of claim 15 are analyzed above in claim 11, and Usui discloses: wherein the second integer value generate at the status register is Y_1 (column 5, lines 53-56, column 6, lines 7-11).

With respect to claims 27-28, 31 are analyzed similarly to claims 11-12, 15 above.

8. Claims 17, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tonks et. al., (U.S. 6,121,816) in view of Usui (U.S. 6,469, 583) as applied to claim 11, and in view of Janesch et. al., (U.S. 6,650,721).

With respect to claim 17, all of the limitations of claim 17 are analyzed above in claim 11, except for: wherein the digital phase locked loop further comprises a

numerically-controlled oscillator, a fourth divider, a phase comparator, and a low-pass filter for producing a locally generated reference clock signal.

In the same field of endeavor, Janesch et. al., disclose: the digital phase locked loop further comprises a numerically-controlled oscillator, a fourth divider, a phase comparator, and a low-pass filter for producing a locally generated reference clock signal (Fig. 1, DPLL, NCO element 114, a divider element 116, a phase comparator (phase detector element 106), low-pass filter (loop filter 110), producing fdds signal, column 4, lines 36-53).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement the DPLL of Tonks et. al., as the DPLL of Janesch et .al., since it exhibits fast settling times (Janesch et. al., column 3, lines 28-30).

With respect to claim 33, claim 33 is analyzed similarly to claim 17 above.

Allowable Subject Matter

8. Claims 13-14, 16, 18-19, 21-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nagaishi et. al. (U.S. 6,747,488) discloses selecting from two frequency sources as an input to a PLL .

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
9/15/2006

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER